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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,747	10/30/2003	Chih-Ching Chen	3722-0168P	6168
2292	7590 08/11/2005		EXAMINER	
BIRCH STEWART KOLASCH & BIRCH			COX, CASSANDRA F	
PO BOX 747 FALLS CHUR	RCH, VA 22040-0747		ART UNIT PAPER NUMBER	
111220 01101	,		2816	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	- N				
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Office Action Summary	10/695,747	CHEN ET AL					
onice Action Summary	Examiner	Art Unit					
The MAIL INC DATE of this communication of	Cassandra Cox	2816					
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet wit	in the correspondence addr	ess				
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a rid.  - If NO period for reply is specified above, the maximum statutory period.  - Failure to reply within the set or extended period for reply will, by stat.  Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	I. 1.136(a). In no event, however, may a re eply within the statutory minimum of thirty od will apply and will expire SIX (6) MON ute, cause the application to become AB	eply be timely filed  (30) days will be considered timely.  FHS from the mailing date of this come  ANDONED (35 U.S.C. § 133).	munication.				
Status							
1)⊠ Responsive to communication(s) filed on 30	October 2003						
	nis action is non-final.						
3) Since this application is in condition for allow		ers, prosecution as to the n	nerits is				
closed in accordance with the practice under	•						
Disposition of Claims	•						
<ul> <li>4)⊠ Claim(s) 1-14 is/are pending in the application</li> </ul>	nn .						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1,2,4,7 and 14</u> is/are rejected.	· <u> </u>						
7)⊠ Claim(s) <u>3,5,6 and 8-13</u> is/are objected to.							
8) Claim(s) are subject to restriction and	/or election requirement.						
Application Papers							
9) The specification is objected to by the Exami	ner						
10)⊠ The drawing(s) filed on <u>30 October 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the			· ·				
Priority under 35 U.S.C. § 119	•						
12)⊠ Acknowledgment is made of a claim for foreig	an priority under 35 H.S.C. &	119(a)_(d) or (f)					
a) ☐ All b) ☐ Some * c) ☐ None of:  1. ☐ Certified copies of the priority docume	·	113(a)-(a) 01 (1).					
2. Certified copies of the priority docume	nts have been received in Ap	oplication No					
<ol><li>Copies of the certified copies of the pr</li></ol>	iority documents have been	received in this National St	age				
application from the International Bure							
* See the attached detailed Office action for a list	st of the certified copies not r	received.					
Attachment(s)	🗀 .	<b>,</b>					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)		ummary (PTO-413) /Mail Date					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/0- Paper No(s)/Mail Date <u>04/05/04</u> .		formal Patent Application (PTO-1	52)				

Application/Control Number: 10/695,747 Page 2

Art Unit: 2816

#### **DETAILED ACTION**

### Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Farwell et al. (U. S. Patent No. 5,731,726).

In reference to claim 1, Farwell discloses in Figure 1 a digital delaying device for delaying an input signal (IN) with digital type, the digital delaying device comprising: a ring oscillator (10) having a plurality of delay cells (N) connected in a loop, for outputting an oscillation clock; a calibration unit (17, 19, 21) for receiving a reference clock (REF) and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period (this is seen to be true when X is equal to one), the pulse number serving as a period reference pulse number (see column 3, lines 1-18); at least one delay number calculation unit (23) for receiving the period reference pulse number and a signal delay value ( $K\tau$ ), calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal (see column 3, lines 54-62); and at least one delay channel (11) comprising a plurality of cascaded delay cells (see Figure 2), the cascaded delay cells receiving an input signal (IN), generating a plurality of delay signals with

Art Unit: 2816

different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal.

In reference to claim 14, Farwell discloses in column 2, lines 38-41 that the delay cells of the ring oscillator (10) and the delay cells of the delay channel (11) have the same delay timing.

3. Claims 1 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U. S. Patent No. 6,025,745).

In reference to claim 1, Lee discloses in Figure 2 a digital delaying device for delaying an input signal (INPUT SIGNAL) with digital type, the digital delaying device comprising: a ring oscillator (31) having a plurality of delay cells connected in a loop, for outputting an oscillation clock (32); a calibration unit (34) for receiving a reference clock and the oscillation clock (32) and calculating a pulse number of the oscillation clock corresponding to each reference clock period (Lee discloses in column 4, lines 45-49 that the time period is selected based on the application, therefore it could be chosen to be a reference clock period), the pulse number serving as a period reference pulse number (38); at least one delay number calculation unit (36) for receiving the period reference pulse number and a signal delay value (NOMINAL PULSE COUNT VALUE), calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal (40); and at least one delay channel (22) comprising a plurality of cascaded delay cells (24), the cascaded delay cells receiving an input signal (INPUT SIGNAL), generating a plurality

of delay signals (26) with different delay timings, and selecting and outputting one of the delay signals as an output signal (29) according to the selection signal.

In reference to claim 14, Lee discloses in column 4, lines 35-36 that the delay cells of the ring oscillator (30) and the delay cells of the delay channel (22) have the same delay timing.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 4, 7, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. Patent No. 6,445,661).

In reference to claim 1, Wu discloses in Figure 5 a digital delaying device for delaying an input signal (EFM) with digital type, the digital delaying device comprising: a ring oscillator (84) having a plurality of delay cells (92-96) connected in a loop, for outputting an oscillation clock; a calibration unit (78, 86, 88) for receiving a reference clock (System Clock) and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period, the pulse number serving as a period reference pulse number; at least one delay number calculation unit (102) for receiving the period reference pulse number and a signal delay value (Delay Enable), calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal; and at least one delay channel (104, 106) comprising a plurality of cascaded delay cells (112-116), the cascaded delay cells receiving an input signal (EFM), generating a

Art Unit: 2816

plurality of delay signals with different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal.

In reference to claim 2, Wu discloses in column 5, lines 13-14 that the frequency of the oscillation clock is higher than that of the reference clock.

In reference to claim 4, Wu discloses in Figure 8 wherein the loop of the ring oscillator (84) further comprises a NAND gate (132) for receiving a reset signal (Control) to reset the ring oscillator (84).

In reference to claim 7, Wu discloses in Figure 5 wherein the calibration unit comprises: a pulse generator (78) for receiving the reference clock (System Clock) and generating a trigger signal (Clear Count) at a rising edge of the reference clock; a counter (86) for receiving the trigger signal and the oscillation clock, the trigger signal (Clear Count) serving as a clear signal; and a register (88) for storing a count value of the counter (86), which serves as the period reference pulse number, according to the trigger signal.

In reference to claim 14, Wu discloses in column 5, lines 40-45 that the delay cells of the ring oscillator (84) and the delay cells of the delay channel (104) have the same delay timing.

## Allowable Subject Matter

5. Claims 3, 5-6, and 8-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Page 6

Art Unit: 2816

6. The following is a statement of reasons for the indication of allowable subject matter: Claim 3 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the circuit further comprises a flip-flop (35) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 5 would be allowable because the closest prior art of record fails to disclose a ring oscillator further comprising a NOR gate in combination with the rest of the limitations of the base claims and any intervening claims. Claim 6 would be allowable because the closest prior art of record fails to disclose a circuit wherein the calculation unit has a calculation function of F(m,M,C)=(m/M)\*C in combination with the rest of the limitations of the base claims and any intervening claims. Claims 8-13 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein the calculation unit includes a first frequency divider (321) in combination with the rest of the limitations of the base claims and any intervening claims.

#### Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

Art Unit: 2816

Page 7

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

August 5, 2005

MY-TRANG NU TON PRIMARY EXAMINER

8/8/05